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Space Power Technology in Power Management and Distribution Electronics

Kitt C. Reinhardt* and Clay S. Mayberry†
U.S. Air Force Research Laboratory, Kirtland Air Force Base, New Mexico 87117
and
Dave S. Glaister‡
The Aerospace Corporation, Albuquerque, New Mexico 87119

Significant advancements in the development of lightweight, compact, reliable, and cost-effective electrical power system components are required to enable high-power designs of future generations of satellites. The goal of the U.S. Air Force Phillips Laboratory is to minimize the cost impact of high-power missions by reducing electrical power system mass to 10% of the satellite mass, thereby allowing the use of smaller launch vehicles. By designing payload power converters to operate at higher frequencies and incorporating state-of-the-art packaging techniques, the specific power of payload power converters will reach greater than 100 W/kg and 3 W/cm^3, with substantially increased radiation hardness. Operating these converters at higher input voltage (120 V) will significantly reduce harness mass for higher power missions. This same technology has also benefitted battery charging and discharging units, solar array power regulation devices, and switching and fault protection devices. Finally, high-temperature wide band gap devices were found to reduce the overall satellite mass by eliminating heaters for worst-case cold environment and by reducing the size of radiator components for hot environments.

Nomenclature

A_r	= thermal radiator area, m^2
E_c	= breakdown electric field strength, V/m
E_g	= semiconductor bandgap, eV
F	= effective radiative interchange or view factor
f	= frequency, Hz
I_L	= junction leakage current, A
k	= Boltzmann's constant
M_C	= harness cable mass
n_i	= intrinsic carrier density
P_T	= total delivered power
Q	= energy per unit time
Q_{htr}	= required operating heater power
$Q_{\min}$	= minimum satellite power dissipation
QR_{minmax}	= ratio of the minimum to maximum operating power dissipation
T	= temperature
$T_{\max}$	= maximum operating box baseplate temperature, K
$T_{\min}$	= minimum operating box baseplate temperature, K
$T_{s\,\max}$	= maximum (hot case) effective radiation sink temperature, K
$T_{s\,\min}$	= minimum environmental sink temperature, K
ε	= emissivity
σ	= Stefan–Boltzmann constant ($5.67e$-8 W/m^2/K^4)

Subscripts and Superscripts

c	= critical
g	= gap
htr	= heater
i	= intrinsic
l	= leakage
max	= maximum
min	= minimum
s max	= maximum heat sink
s min	= minimum heat sink
1	= electronic box 1
2	= electronic box 2

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*FTA Manager, Power and Thermal Group, Phillips Research Site. E-mail: reinhark@plk.af.mil.

†Solar Thermal Program Manager, Power and Thermal Group, Phillips Research Site. E-mail: mayberry@plk.af.mil.

‡Program Engineer, U.S. Air Force Research Laboratory, Phillips Research Site, P.O. Box 9045. E-mail: glaister@kafb.aero.org.

Introduction

TO meet the demand for increased satellite payload mass and power and to reduce launch vehicle size and cost, an increasing amount of attention is being given to the satellite electric power system (EPS) performance in terms of specific power, size, stowed volume, and cost. The EPS is responsible for providing uninterrupted, fault-tolerant electrical power to satellite payload and housekeeping equipment throughout the lifetime of the mission. Satellite EPS size (power level) is dictated by payload characteristics such as antenna power, data rate, and satellite orbit. Typical power levels and mass of today's satellites range between 100 and 1000 W and 250 kg or less for small satellites, to between 1 and 10 kW and on the order of 1000–5000 kg for conventional large satellites. However, due to present shrinking space budgets, mission planners are pushing strongly toward cheaper, small-satellite designs capable of launch on smaller, cheaper, and more easily deployed vehicles. For example, the U.S. intelligence community has recently evaluated requirements for future surveillance missions and has acknowledged the advantages of lower cost small satellites to address tomorrow's war fighter needs. These needs include increased flexibility, improved performance, and the ability to launch satellites easily when needed. In contrast, mission planners have also acknowledged the need for significantly larger 10–50 kW monster satellites to enable next-generation communications, radar, and weapons platform functions. Prime contractors have projected communications satellite power needs reaching 15–20 kW in the next five years, and military platform power needs are projected to exceed 50 kW over the next decade.

Resulting EPS design challenges for future small and monster satellites are similar in some respects. In the case of small satellites, the goal is to increase EPS specific power to help reduce total satellite bus mass and volume to allow increased payload capability and use of smaller, cheaper launch vehicles. In the case of monster satellites, the paramount challenge is to increase EPS specific power to enable sufficient power growth while maintaining acceptable satellite mass and volume to allow use of existing launch vehicles. For example, the largest U.S. military system that has recently been launched is

the ~8.6-kW Milstar satellite having a dry mass of 4417 kg. Milstar was placed in orbit by the largest U.S. heavy-launch vehicle, the Titan IV, having a maximum geosynchronous transfer orbit (GTO) lift capability of ~4540 kg. Hence, excluding the Space Shuttle, state-of-practice large satellites have already reached maximum-lift capabilities. This poses an even greater challenge for launching future monster satellites with power levels of approximately 10 kW. To take advantage of significantly reduced launch costs, satellite designers are also pushing for utilization of smaller medium-launch vehicles, such as the Atlas IIAS with a GTO payload capability of ~3677 kg and a cost of $\$20.4 \times 10^3$/kg vs $\$37.4 \times 10^3$/kg for the Titan IV. The Atlas IIAS is capable of launching state-of-practice ~6 kW and next-generation 8–12 kW satellites.

To meet projected small- and monster-satellite design requirements, revolutionary advancements in EPS component technology are required over today's conventional technologies. A typical satellite EPS [solar array and support mechanisms, batteries, power management and distribution (PMAD) electronics, and PMAD cabling/harness] utilizing state-of-practice technology accounts for about 20–30% of the total satellite mass and occupies a significant portion of the satellite volume. A breakout of average EPS component mass for the operational Defense Satellite Communication System III (DCSCIII), Defense Support Program (DSP), Global Positioning Satellite (GPS), and Milstar satellites is shown in Fig. 1. For these satellites, the EPS-to-total satellite mass percent of 20–30% corresponds to measured EPS specific power values of 3–5 W/kg (Ref. 1).

The goal is to increase total EPS specific power through advancements in component technology to enable a reduction in EPS mass percentage to ~10%. A complement of ongoing EPS technology development programs at the U.S. Air Force Phillips Research Site (PRS) promises to increase EPS specific power to 10 W/kg by fiscal year (FY) 2000 and 13 W/kg by FY2005. In short, development programs in energy storage at PRS include NaS, Li-ion, and Li-polymer electrochemical storage cells and mechanical flywheels that promise a 2–3 times improvement in energy capacity (specific energy, watt-hour per kilogram) over state-of-the-art NiH_2 batteries.[2] Technology development in energy generation includes 24–26% efficient three-junction $GaInP_2$/GaAs/Ge and 30–32% efficient four-junction $GaInP_2$/GaAs/GaInAs/InP multijunction solar cells, and 30–35% efficient alkali metal thermal to electric converter solar thermal converters. These technology improvements promise a 40–70% reduction in energy generation system mass over state-of-the-art GaAs solar arrays.[1,2]

As shown in Fig. 1, the mass of PMAD electronics and harness (cabling, shielding, and connectors) account for 25–35% of the total EPS mass. Ongoing technology efforts at PRS in PMAD are focused on increasing PMAD circuit efficiency and modularity/packing density to reduce mass and volume,[3] increasing PMAD bus voltage to substantially reduce PMAD harness mass, and increasing maximum PMAD box operating temperature to help reduce the mass and power consumption of satellite thermal control systems. An increase in PMAD efficiency will also yield reductions in solar array and thermal control system size and mass due to reduced PMAD power loss and heat dissipation, respectively. The following sections discuss the basic satellite PMAD architecture, benefits of increasing PMAD system voltage, efficiency and operating temperature, and the status of ongoing PMAD development programs.

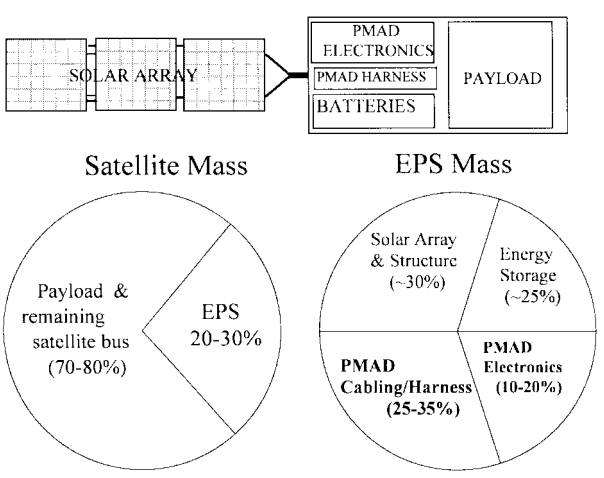


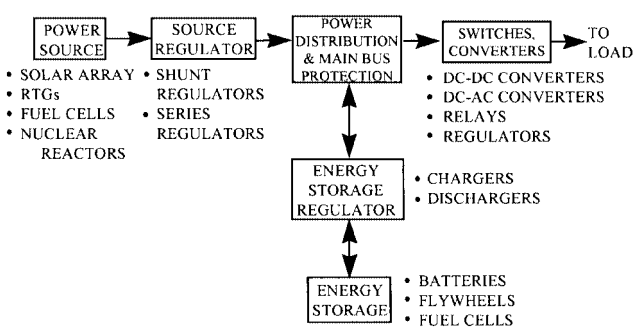
Fig. 1 Satellite EPS components and component mass fraction averaged for state-of-practice DSCSIII, DSP, GPS, and Milstar satellites.

Trends in Satellite PMAD Development

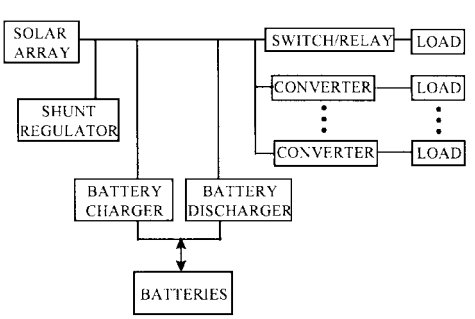
The function of the satellite PMAD system is to regulate, control, monitor, and distribute electrical power between the satellite solar array, storage batteries, and loads (payloads). The regulation/control system regulates electrical power generated at the solar array to prevent battery overcharging, regulates the bus voltage, and charges and discharges the battery. The distribution system consists of a cable harness to interconnect EPS components and loads, fault protection to detect and isolate faults, and relay and power converter switches to turn power on and off to the loads. A schematic showing a generic satellite EPS architecture with various EPS component technology candidates and a configuration for a fully regulated PMAD bus utilizing shunt regulation is shown in Fig. 2.

Solar Array Regulation

Nearly all Earth-orbiting satellites rely on solar arrays and electrochemical batteries for energy generation and storage, respectively, because of mass, cost, reliability, and safety considerations. Solar array power must be controlled by a regulator unit to prevent battery overcharging and undesired satellite heating. Two common regulation techniques are peak-power tracking (series regulation) and direct-energy transfer (shunt regulation). In peak-power tracking (PPT) a dc–dc converter dynamically changes the solar array operating point to extract the exact power required for battery charging and payload needs. PPT can also extract the maximum power generated by the array, and state-of-the-practice PPT unit efficiencies range from ~90 to 95%. Because PPT power losses are low and because it is capable of extracting a large amount of power at beginning-of-life (BOL) and when the array is cold (posteclipse), it is desirable for short, low-Earth-orbit (many eclipses) and severely power-limited missions, e.g., radar mapping and small experimental satellites. Conversely, many communication, weather, and navigation satellites have relatively constant BOL vs end-of-life (EOL) power requirements and are designed to use the solar array EOL capability. If the satellite cannot be designed to optimally use solar



a) Generic satellite EPS configuration



b) Fully regulated satellite PMAD system

Fig. 2 Block schematics.

array BOL power, there is no benefit to using PPT. Further, it was concluded that the amount of additional power obtainable when the array is cold may only be important for body-mounted solar arrays that have sufficiently large mass that result in a long enough delay time before the array reaches sunlight temperatures. For those systems employing PPT, increased controller efficiency is desired to reduce both the size of the solar array and thermal control system through reduced power and heat dissipation, respectively.

In direct-energy transfer (DET), the regulator operates in parallel with the solar array and shunts extra power (current) either at the array or to external resistor banks to meet battery and payload needs. DET shunt regulation is designed to maintain the solar array EOL power level on the bus by shunting a large amount of solar array excess power at BOL. The parallel configuration of DET regulation eliminates the 5–10% power loss of PPT regulation and, hence, results in higher total system EOL efficiency for long, high-power, e.g., large and monster satellite, missions. Additional advantages of DET over PPT include fewer parts, lower cost, and lower mass. Although improving DET regulator efficiency is inconsequential, significant reductions in regulator mass can be achieved using advanced high-density hybrid circuit and packaging technologies.[3]

Power Distribution Bus

The power distribution design is driven by the satellite power level and load regulation requirements. As satellite power levels increase to satisfy large-satellite (5–10 kW) and monster-satellite (>10 kW) needs, power distribution cable losses and limits on harness mass demand the use of higher voltage buses. Significant savings in PMAD harness mass can be achieved at higher bus voltages because less current is required to deliver equal power, resulting in smaller or fewer cables. The harness cable mass varies inversely with the square of the bus voltage V according to the relation $M_C \propto (P_T/V)^2$. This relationship between M_C and V can result in significant harness mass reduction. Conventional satellite power distribution has relied on a standard 28-V dc bus and standard 28-V dc electronic components for over 30 years. Table 1 illustrates the trend toward higher voltage (50–100 V dc) bus designs for large satellite geosynchronous Earth orbit (GEO) systems.

To illustrate the effect of increasing bus voltage on harness mass, consider the Milstar satellite, which currently employs a ~28-V dc bus with an EPS mass of greater than 844 kg, 230 kg due to wiring harness and 167 kg due to PMAD box (shunt regulator, battery charger/discharger, payload regulator) mass. The calculated savings in Milstar PMAD harness mass using 70- and 100-V distribution would be 70 and 88 kg, respectively. The savings in PMAD cable mass (excluding connectors) for a generic regulated-bus large satellite is shown as a function of distribution voltage in Fig. 3. The savings in mass is shown to begin for power levels >2 kW and to significantly increase at higher power levels. The benefits of high-voltage PMAD systems are understood. However, the primary challenge remaining is the availability of suitable high-voltage PMAD components. There are presently no off-the-shelf space-qualified, commercially available high-voltage converters or switches rated for >60-V dc operation. It is anticipated, however, that as power levels increase, spacecraft component and bus designers will pursue and adopt high-voltage bus shemes.

Table 1 Trends in satellite system power and voltage

Satellite system	Power, kW	Bus voltage, V dc
Hughes 601	8	50
Hughes 702	15	100
Space systems/Loral	8	100
Lockheed Martin A210	6	70
Space station	To be determined	120

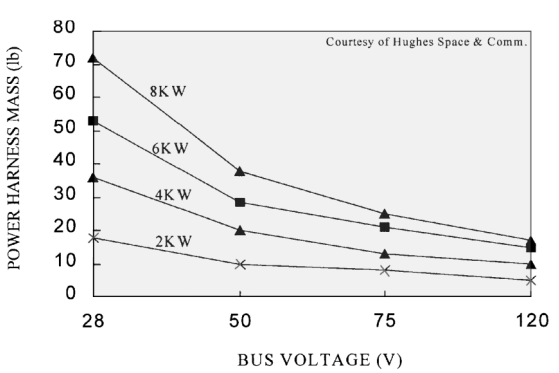


Fig. 3 Power harness mass vs power bus voltage.

Battery Charge/Discharge Units and Power Bus Regulation

The design of the battery charge and discharge architecture depends on the satellite mission. A battery charging unit (BCU) is required to charge the battery when in sunlight, and in a fully regulated bus architecture, a battery discharge unit (BDU) is used to both transfer power from the battery and regulate the bus voltage during eclipse. This architecture is shown in Fig. 2b. For BDU and BCU functions, dc–dc converters are commonly used, and their efficiencies range as high as ~95%. Regulated bus voltage distribution is generally favored over unregulated distribution for GEO missions (which encounter very few eclipse periods) to optimize payload power converter efficiency and minimize converter mass. Payload power converter efficiencies range from 85–90% for a regulated bus to 60–80% for an unregulated bus. In the case of the unregulated bus, the battery is connected directly to the bus, and the bus voltage equals the battery voltage, which can vary about 20% between battery charge and discharge. The varying bus voltage results in the reduced payload converter efficiency and a significant mass penalty due to added electronics (added power consumption) and input filter complexity. However, for low-Earth-orbit missions that experience ~6000 cycles/year, the ~5% BDU power loss each cycle is prohibitive, and the unregulated bus design is desirable. Because very few battery charge/discharge cycles occur in GEO, the 5% BDU power loss is inconsequential. Increased BCU and BDU efficiency is desired to help reduce both the size of the EPS solar array and thermal control system through reduced power loss and heat dissipation, respectively. Further, significant reductions in unit mass and volume can also be achieved using advanced high-density hybrid circuit and packaging technologies.

Payload Power Converters

The efficiency of payload power converters is critical to overall PMAD efficiency. The design of payload power converters is determined by the payload power profile. Predominant satellite payload functions (communications, radar, computers, and motors) require a wide range of input voltage levels, converted from the bus voltage using dc–dc and dc–ac converters. Typical payload input voltages include ~3–270 V dc, high-voltage single-phase ac (115 V rms, 60 Hz) or high-voltage three phase ac (120/440 V rms, 400 Hz). Payload power converter size and efficiency depend on the type of bus regulation, as well as on the load input voltage. The use of a regulated bus allows improved efficiency and reduced converter unit mass because the converter can be optimized (requiring fewer components and less power) for single-voltage conversion. State-of-the-practice payload dc–dc converter efficiencies range between ~85–90% and ~60–80% for regulated and unregulated voltage distribution, respectively.

Digital electronic systems compose a significant percentage of satellite loads. Power losses in digital systems are proportional to the product $V^2 f$. As payload clocking frequencies continue to increase to enhance electronics processing capability, designers are reducing payload input voltages to maintain acceptable power losses. This reduction in payload input voltage has an effect on converter efficiency due to the competing converter output stage diode voltage drop. This inevitably reduces converter efficiency and increases converter complexity, mass, and cost.

The impact of payload power converter efficiency, as well as battery charger/discharger unit efficiency, on total PMAD efficiency and power dissipation is shown in Fig. 4. Depending on the number of loads and the mission profile (number of eclipses), a worse-case calculation results in a ~20% power loss due to regulator inefficiencies. This power would typically be dissipated by the

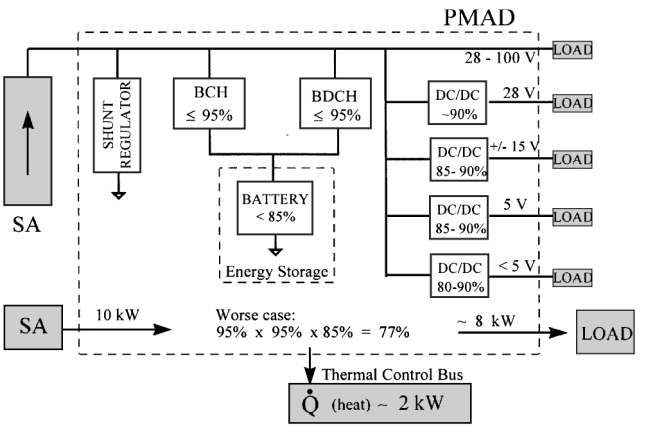


Fig. 4 Schematic of fully regulated PMAD system showing converter/regulator inefficiencies.

satellite thermal control system, which can typically weigh ~0.5 kg per 10 W of dissipation. Hence, increased converter/regulator efficiency will help reduce the size of both the solar array and thermal control system through reduced power consumption and heat dissipation, respectively. Power converters are also important for isolating (filtering) both bus noise from the load and load-generated transient noise from the bus.

Switches for Fault Isolation

The fault tolerance of the PMAD system is of paramount concern. Satellite PMAD boxes typically require relays and/or fuses for on/off control and current sensors for fault management and control. Fault isolation is usually provided by relays and fuses; fuses open overcurrent paths, and relays select a new path. Present power relays are limited to mechanical magnetic latching devices because of their proven reliability and low-power dissipation. However, relays have a number of application problems, including susceptibility to inrush current resulting in contact arcing and welding at high-power levels. Relays also have no feedback telemetry and exhibit poor temperature stability, and high-voltage relays are heavy. The goal is to replace the mechanical relay, fuse, and sensor combination with a single intelligent solid-state switch (SSS) capable of both load switching and fault isolation. The switch would be a one-for-one replacement for the relay combination and have a serial interface enabling the satellite computer to monitor and control the switch turn-off current. Similar switching capabilities are commercially available for terrestrial use, but there are presently no off-the-shelf space-qualified SSSs.

Advanced PMAD Component Development

A U.S. Air Force-sponsored study was recently conducted to determine the status of existing military, commercial, and NASA satellite PMAD technology efforts and to recommend new technology developments needed to support next-generation Air Force satellite mission requirements.[1] Study objectives focused on identification of ongoing research and development (R&D) efforts, determination of Air Force program office needs and requirements, and most importantly recommendations for new technology development that can increase PMAD specific power (watt per kilogram) by a factor of 2–3 times. Although emphasis was placed on identifying PMAD component technologies that were feasible to develop, qualify, and deploy within the next 5–10 years, a number of longer range technology opportunities were also identified. Results from these PMAD studies fall within two categories: system level and component level. System-level studies identified 1) the benefits of dc power distribution over ac distribution, which are simpler architecture and less costly; 2) the benefits of high-voltage power distribution and need for new high-voltage bus standardization to reduce PMAD harness mass and volume; 3) the advantages of regulated PMAD power distribution to reduce payload power converter size, mass, and efficiency losses; and 4) the benefits of DET solar array regulation over PPT regulation, which is greater EOL efficiency for most missions.

Component-level studies identified a need for a new family of PMAD component development. Specific recommendations include a need for 1) space-qualified, radiation resistant high-voltage (45–130 V dc) power converters with performance goals of >92% efficiency, >100 W/kg, and >3 W/cm^3, 1–10 A; 2) space-qualified, radiation resistant high-voltage (45–130 V dc) SSS to provide a one-for-one replacements for relay/fuse combinations with performance goals of >99% efficiency, >440 W/kg, >3 W/cm^3, >5 A, current telemetry, fault tolerance, and resettable; 3) battery cell bypass switches to enable single-battery bypass instead of redundant batteries with performance goals of 200 A and <200 g, 4) high-efficiency (low-voltage drop), 100-V, 200-A diodes for switching power components within the PMAD system; 5) standard/flexible battery charge control unit capable of charging nickel cadmium, nickel hydrogen, nickel metal hydride, lithium/lithium ion, and lead acid batteries; and 6) radiation resistant, >5-A power transistors [metal oxide semiconductor field-effect transistor (MOSFET) or insulated gate bipolar transistor]. Increased space qualification of existing commercial electronic devices (active and passive) is needed. Device testing and rating for high voltage (acceptable voltage derating is ~30–40%), temperature, and radiation resistance, etc., is very expensive, and many traditional space electronics vendors have discontinued space-qualified device product lines because of the relatively small commercial market that demands them.

Additional recommendations include a need for power electronics standardization. For example, Hughes Electronics Corp., Loral, Lockheed Martin Astronautics, and others are making significant efforts to ensure that PMAD units are being developed that are usable on a variety of programs. Common hardware designs are desired for multiple programs to reduce nonrecurring cost and cycle times. Also, hybridization and modularization of power electronics is recommended to reduce PMAD system mass and volume. As will be discussed, a tremendous reduction in PMAD box size can be realized using advanced multichip module and high density interconnect (HDI) packaging technologies. In the area of advanced semiconductor device development, the ability of wide band gap semiconductors, such as silicon carbide, to operate at both higher temperatures and higher efficiencies over conventional silicon-based devices shows good potential for use in high-temperature (HT) PMAD systems. As will be shown, increasing the maximum allowable PMAD box temperature can result in reducing the size, mass, and power consumption of the satellite thermal control system.

A description of ongoing Air Force PMAD component R&D efforts is given in the following sections. Planned PMAD development efforts are currently divided into two phases. Development of high-voltage (45–130 V dc) payload power converters (PPC) and SSS began in phase I. The main goal of these programs is to produce commercially available, standardized, high-voltage PPC and SSS components. Phase I began in FY1995 and will be completed in FY1998. A series of wide band gap semiconductor device and circuit trade studies were also initiated in phase I to better understand the potential of HT (~250°C), higher efficiency PMAD operation. Several results from these studies will be discussed in turn. The development of much needed battery bypass switches and 200-A high-efficiency diodes was delayed until the start of phase II (FY1999) due to funding constraints. Phase II will also initiate the analysis and development of a first-generation HT space PMAD system design.

Payload dc–dc Converters

There are presently two major high-voltage payload converter development programs underway at PRS, each slightly unique from the other. Virginia Power Technologies (VPT) is developing a high-voltage input, low-voltage output dc–dc converter employing state-of-the-art, radiation hard semiconductors to operate at as high a switching frequency as possible consistent with available magnetic material. By using frequencies as high as 1 MHz, the size of switching magnetics and filter components are reduced. However, circuit efficiency must be maintained because losses translate directly back into an increase in the size and weight of the satellite in the form of heat sinking, battery capacity, solar array size, etc. VPT has achieved power stage efficiencies as high as 92%. Most applications and, therefore, designs have power requirements below 200 W. If

additional power is required, a modular approach is taken; the devices can be paralleled. Hybridization of the design was used to further reduce the overall size of the device. VPT has taken the approach of designing converters with specific applications for Space Systems Loral and Lockheed Martin Astronautics. The input voltages to the converter are regulated and are 90–110 V-bus for Space Systems Loral and 68–71 V for Lockheed Martin Astronautics. The output voltages range from 2.5 to 15 V.

In a parallel effort, TRW Space and Technology Division, Space and Electronics Group, is developing four dc–dc converters operated at a 600-kHz switching rate with unregulated input voltages ranging from 45 to 130 V. Reported efficiencies have ranged from 74 to 89.5% including power losses in housekeeping circuits. The 5-W converters operate in the discontinuous flyback mode, the 10–50 W converter operates in the current-controlled forward mode. All designs share a common layout and use the same control electronics. The converter incorporates hybridized packaging techniques, and the use of higher frequencies have resulted in a reduction in mass and volume.

High-Density Power Electronics

Extensive efforts are being conducted in commercial, military, and space arenas to reduce the mass and volume of PMAD electronics boxes. State-of-the-practice power converters deliver less than 0.6 W/cm^3 and 110 W/kg. However, recent developments in resonant conversion, high-frequency devices, and packaging technologies such as hybrids and HDI technologies are making power conversion densities of 6 W/cm^3 and 660 W/kg. With the exception of device selection, nothing has more profound impacts on the performance of PMAD components than the methodology used for their packaging. Advanced packaging technologies address the efficient arrangement and interconnection of electrical components in a PMAD design to promote the highest performance possible, enabling these designs to approach the theoretical limits associated with the constituent devices. In particular, multichip module (MCM) technologies allow devices to be placed closely to each other, reducing electrical and thermal path lengths, and allow the mixture of device technologies, e.g., Si, GaAs, and SiC. The ability to mix devices is especially important because the key to highest efficiencies in many power convertor topologies is realized by constructing digital controls with efficient complementary metal-oxide semiconductors, whereas other portions of the topology benefit from the introduction of devices with extremely low on-resistance or very high breakdown voltages. Attempting to achieve these features simultaneously in a monolithic integrated circuit (IC) is not practical; hence, many monolithic power convertors compromise some aspects of performance in order to incorporate an entire design onto a single IC.

To achieve near-monolithic benefits and maximum performance, the application of new forms of advanced patterned overlay MCM technology is being explored by PRS,[3] in particular the HDI process. Figure 5 shows the general configurations that are employed using patterned substrate and patterned overlay technologies. Unlike patterned substrate technologies, which mount components onto a substrate with prepatterned interconnections, patterned overlay technologies form a thick, electroplated interconnection manifold directly onto the contact terminals of electrical components. In this manner, traditional wire-bonds are replaced with vias, similar to the approach used to interconnect transistors within an IC, minimizing parasitic resistance, capacitance, and inductance. The minimization of series losses between components is extremely important in PMAD designs. Patterned overlay interconnections achieve this with a robust multilayer Cu (4 μm)/polyimide (25–37 μm) interconnections system, which manifests superior electrical performance when compared to ICs or ordinary hybrid approaches. Patterned overlay MCMs offer greater component densities because minimal floor plan headroom is required (wire bonds require additional lateral space for completing the connection from chip to substrate). Furthermore, the patterned overlay approach separates electrical and thermal paths, allowing independent optimization of electromagnetic and thermal performance.

These salient characteristics of patterned overlay result in improved performance of existing PMAD component architectures,

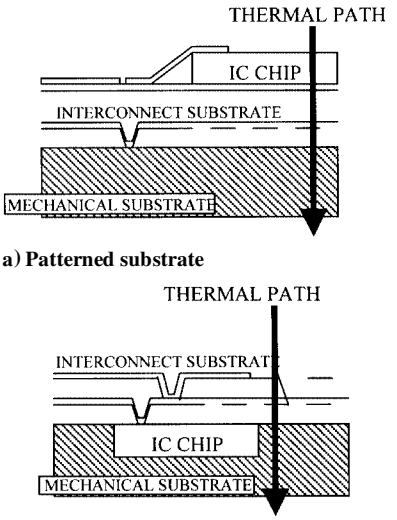


Fig. 5 General MCM configurations.

but more importantly, allow more aggressive topologies in components such as power convertors to be explored. PRS has developed over 50 MCM designs based in patterned overlay technology, with two active programs in power convertor development. The first program, sponsored by the Defense Advanced Research Projects Agency and contracted to General Electric's Corporate R&D Center (Schenectady, New York), is exploring methods of achieving low-cost HDI packaging (for example, plastic substrates replace ceramic) and efficient point-of-load power conversion.[§] Conversion efficiencies as high as 92% are predicted with power conversion densities in excess of 100 W/cm^3. A second program, sponsored by the U.S. Air Force Space and Missile Center and contracted to Lockheed Martin Astronautics (East Windsor, New Jersey), is exploring the development of efficient space-qualified power convertors in the HDI process. This program is currently targeting a conversion density of 660 W/kg, resulting in radiation hardened, credit-card-sized convertors with over 75 W power output. It is a general finding of this research that significant improvements in power convertor performance can be realized through the introduction of optimized packaging technologies.

SSSs

A family of high-voltage (45–72 V and 75–130 V) SSSs is being developed at Rocketdyne Aerospace, a division of Boeing North American, under sponsorship of PRS to replace the relay and fuse combinations now used for isolation and protection of satellite PMAD systems. Like the relay and fuse, the SSS is designed as a component for use in the power distribution system or as protection within individual subsystems. The advantages of the SSS include controlled current rise and fall rates (to reduce bus transients), the ability to limit current (controls inrush current when energizing capacitive loads or cold heating elements), predictable and repeatable trip performance (vs a space-rated fuse), extremely long life (in terms of total operations before wear out), reliability (>95% for 10 years of operation), resetability (vs a cleared fuse), and integral current monitoring (for enhanced power management). An SSS capable of bidirectional current control and isolation (for use as a cross tie in redundant power systems) can be implemented by connecting two unidirectional SSSs in series and using common on/off commands. The disadvantages of the SSS are the higher overhead power consumption (vs latching relay/fuse implementations), slightly higher voltage drop (vs a new contact), single-direction current flow (present designs), and limited radiation tolerance (vs relay/fuse).

The trend toward increasingly higher bus voltages further favors the SSS over the relay/fuse because of the increased difficulty, and

[§]The project description is available at http://esto.sysplan.com/ETO/El-Packaging/Projects/MCI/GE.html.

consequential size and weight penalties, associated with quenching turn-off/clearing arcs of relay contacts and fuse elements. The SSS achieves high switch efficiency (typically greater than 99.5%) by using paralleled power MOSFETs as the switching elements. This approach allows the voltage drop of the switch to be made arbitrarily small by increasing the number of paralleled field-effect transistors (FETs). A tradeoff must be made between voltage drop and the cost, weight, and volume of the switch to determine the best solution for a particular application. The present Rocketdyne Aerospace SSS designs achieve voltage drops equivalent to 0.2–0.5% of the applied bus voltage for two voltage ranges (45–72 and 75–130 V) with specific power and power density levels of 826–6872 W/kg and 2.3–16.5 W/cm^3, respectively, for a current range of 1–10 A. The SSS design is self-powered, drawing 50 mW or less of housekeeping power from the power bus while the switch is in the off state and 0.8 W (at 45 V) to 2.4 W (at 130 V) when the switch is on. The SSSs are designed for a total radiation dose of 100 krad (Si) with a radiation design margin of 2. At present, the SSS design utilizes a hybrid microcircuit for the control/housekeeping functions and some surface-mounted discrete components (including the FETs, output clamp diode, and pulse isolation transformer) on a copper–invar–copper printed wiring board. A significant reduction in the size of the SSS can be achieved by combining all of the SSS components in a single hybrid circuit. A number of 45–75 V (3 A) and 72–130 V (1, 10 A) SSS engineering qualification units are scheduled for delivery to PRS in November 1998.

Potential of HT Space PMAD Systems

Impact of HT PMAD on Satellite Thermal Control System

The impact of using HT electronics onboard a generic low-Earth-orbit (LEO) and a Milstar class GEO spacecraft was evaluated using a simplified thermal model. This evaluation resulted in a first-order assessment of the mass and power savings that would result in the spacecraft's thermal system due to the larger operating temperature range of the SiC components relative to conventional Si-based electronics.

Simplified Spacecraft Thermal System Model

The impact of the temperature range and power of the satellite electronics package was analyzed using a simple two-node thermal model. This simple model is only approximate as a detailed model with numerous nodes, which includes thermal capacitances and resistances required for accuracy. Basically, the required radiator surface area is determined by the maximum dissipation at the maximum operating temperature in the worst-case hot environment. Then, the required heater power can be determined by the necessary supplemental heat required to maintain the minimum operating temperature during the minimum-power dissipation at the worst-case cold environment. For this model, the following equation provides the required radiator surface area for heat rejection to space:

$$A = \frac{Q_{\max}}{\sigma \times \varepsilon \times F \times \left(T_{\max}^4 - T_{s\max}^4\right)} \tag{1}$$

for either the maximum operating box baseplate or maximum (hot case) effective radiation sink temperature. Thus, the following equation provides the ratio of radiator surface areas for two different electronics boxes in the same space environment:

$$\frac{A_1}{A_2} = \frac{Q_{\max 1} \times \left(T_{\max 2}^4 - T_{s\max}^4\right)}{Q_{\max 2} \times \left(T_{\max 1}^4 - T_{s\max}^4\right)} \tag{2}$$

The required operating heater power can be determined by the following relationship:

$$Q_{\text{htr}} = A \times \sigma \times \varepsilon \times F \times \left(T_{\min}^4 - T_{s\min}^4\right) - Q_{\min} \tag{3}$$

Substituting in the radiator area from Eq. (1), the following relationship results:

$$Q_{\text{htr}} = Q_{\max} \times \left[\frac{\left(T_{\min}^4 - T_{s\min}^4\right)}{\left(T_{\max}^4 - T_{s\max}^4\right)} - QR_{\text{minmax}}\right] \tag{4}$$

Table 2 Sink temperatures for LEO and GEO orbits

	Sink temperature, K	
Orbit	Minimum	Maximum
LEO	200	250
GEO	200	215

Table 3 Electronics baseplate temperature ranges

	Baseplate operating temperature, °C	
Electronics	Minimum	Maximum
Si generic LEO	−10	50
Si Milstar GEO	10	40
SiC	20	180

Table 4 Baseline mass and power for spacecraft and thermal control system

	Power, W		Mass, kg	
Electronics	Spacecraft	Thermal system	Spacecraft	Thermal system
Generic LEO	3000	300	2000	120
Milstar GEO	3700	640	3000	330

The effective radiation or environmental sink temperatures for generic LEO and GEO spacecraft were developed using some simplified combined solar, Earth, and Earth reflection flux models in combination with empirical experience and are listed in Table 2. These sink temperatures are only an approximation as a detailed analysis is required for accuracy that takes into account the exact orbit parameters, the spacecraft attitude and orientation, and the surface geometries where the boxes are located.

Overall, the use of the simplified thermal model in combination with the generic sink temperatures is probably only accurate to within 25%. However, this accuracy is sufficient for this first evaluation of the impact of SiC electronics on the thermal control system.

Electronics Temperature Ranges

As shown in Eq. (1), the electronic box baseplate (not piece part or chip) temperature range is required to size the thermal control system. Based on data for a range of boxes on the Milstar GEO and several LEO spacecraft, a generic typical Si-based electronic box baseplate temperature range was determined. For the SiC electronics, a similar temperature gradient to the Si boxes was assumed between the chips and the baseplate. This was combined with test data on SiC to generate a range for the baseplate temperatures. This range was narrowed slightly to easily fit within the operating range of methanol heat pipes to allow for transportation of heat over a distance on the spacecraft. It should be noted that methanol heat pipes are a relatively proven technology with space flights on several spacecraft including Milstar. The resulting estimates for the electronics baseplate temperature ranges for Si in LEO and Milstar class GEO orbits and SiC are provided in Table 3.

Baseline Spacecraft Thermal Control Systems

Based on historical mass property and power data, baseline mass and power for the spacecraft and the thermal control system were estimated for a generic LEO and a Milstar class GEO spacecraft. The baseline estimates are given in Table 4.

Impact of SiC-Based Electronics on Spacecraft Thermal Control System

Based on the preceding thermal model, sink temperatures, electronics baseplate temperatures, and the baseline spacecraft and thermal systems, the impact of incorporating wider operating temperature SiC in all or a portion of the electronics was evaluated. Figure 6 is a plot of the required minimum operating power dissipation ratio to prevent the need for heater power as a function of the maximum electronics operating temperature. The figure indicates that for both a LEO or GEO orbit, SiC-based electronics would only

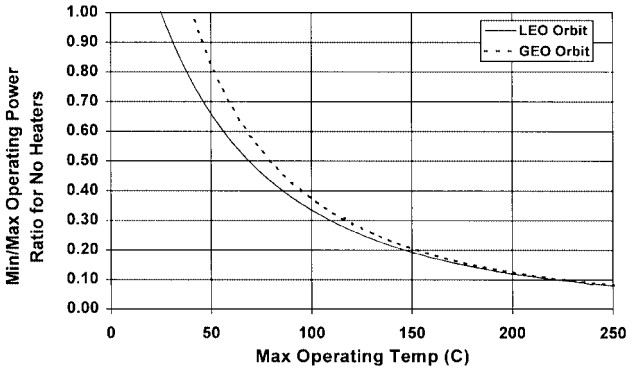


Fig. 6 Minimum operating power for no heaters and 20°C minimum operating temperature.

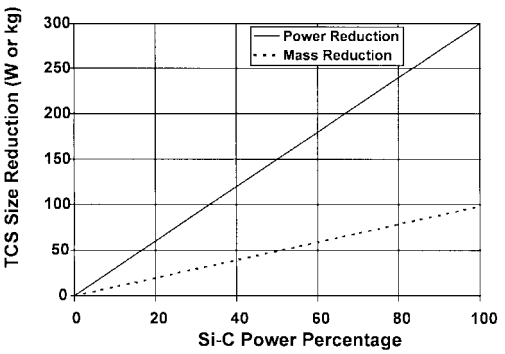


Fig. 7 SiC-thermal control system impact on generic LEO spacecraft size or mass.

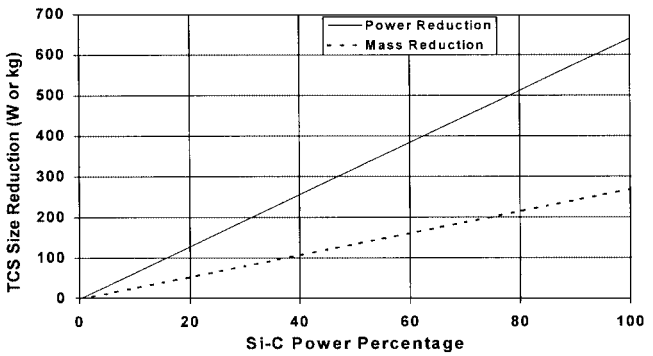


Fig. 8 SiC thermal control system impact for Milstar class GEO spacecraft.

need at least 20% of the maximum power dissipation for the minimum power dissipation modes to avoid using any heater power. Because the minimum power dissipation is typically substantially higher than 25%, heaters would probably not be required on SiC-based electronics boxes. This conclusion was used to estimate the savings in thermal control system power (or heaters) as a function of the total portion of SiC-based electronics. This power savings is shown in Figs. 7 and 8 for a generic LEO and a Milstar class GEO spacecraft. The savings is very substantial as, for a best-case scenario of 50% SiC-based electronics, the reduction in power usage is about 150 W for the LEO spacecraft and over twice that for the GEO spacecraft.

The relative radiator size requirements for the Si- and SiC-based electronics were used to ratio the mass of the spacecraft thermal system. Though only an approximate estimate, this ratio is based on the radiators being typically the heaviest thermal system component and drive the sizing of the remainder of the system. The estimated thermal system mass reduction for a generic LEO and a Milstar class GEO spacecraft is shown in Figs. 7 and 8. The mass savings is also substantial as, for a best-case scenario of 50% SiC-based electronics, the reduction in thermal mass alone is about 50 kg for the LEO spacecraft and almost 150 kg for the GEO spacecraft.

HT Wide Band Gap Semiconductor Devices

For over 40 years, developments in solid-state electronics have provided the U.S. military with the most sophisticated and capable air, space, and terrestrial platform electronic systems in the world. Whereas conventional Si-based solid-state devices have continually been the workhorse of microprocessors, digital signal processing, large memory, analog I/O, and power control electronics, a significant amount of interest has recently been generated in wide band gap (WBG) semiconductors such as silicon carbide for advantageous use in HT, high-power, high-frequency, high-radiation, and nonvolatile device applications.[4] WBG solid-state devices are capable of operating at higher temperatures, higher power levels, and at greater efficiencies compared to a Si-based device. Consequentially, they have tremendous potential for use in a myriad of military and commercial electronic system applications. The U.S. Army and Navy, and the commercial automobile industry have similarly identified significant advantages of utilizing WBG electronics in next-generation technology applications. However, the impact of WBG-based electronics on satellite PMAD system performance has not yet been analyzed.

The traditional maximum operating temperature for low-power Si ICs is limited to temperatures below 200°C. In the case of high-power Si devices, the maximum temperatures drops significantly due to high electric-field effects. To maintain device reliability and longevity, the current maximum MIL-STD temperature for Si-based devices is 125°C. In the past, Department of Defense system development directives have even specified a maximum Si-device junction temperature of 110°C to ensure reliability, and several recent major aircraft programs have limited Si-device junction temperatures to less than 70°C to yield major reliability improvements. WBG are capable of reliable operation at higher temperatures than Si devices because WBG devices generate both smaller semiconductor intrinsic carrier densities and reverse-biased junction leakage currents at elevated temperatures. The value for n_i increases exponentially with temperature as $\exp(-E_g/2kT)$. At sufficiently HTs, the value of n_i will exceed the semiconductor doping density, and the p/n diode junction will be washed out. However, the temperature at which this occurs for SiC with $E_g \sim 3.3$ eV is >1000°C, and the factor that limits maximum device temperature turns out to be device leakage current. Device junction leakage current also increases exponentially as $\exp(-E_g/2kT)$. The device temperature must be limited to maintain a sufficiently small value of I_L, such that the ratio of device on-current $(I_{on})/I_L > 10^5$–10^7. It is clear from the exponential relation that semiconductors with larger E_g will have smaller leakage currents and will enable higher temperature operation. From the exponential relation, SiC with $E_g \sim 3.3$ eV should be capable of operation at ~3 times greater temperatures than Si devices with $E_g = 1.1$ eV. Further, a maximum acceptable device leakage current of 0.1 A/cm^2 was defined by Zipperian et al.,[5] and semiemperical data obtained for HT SiC rectifiers yielded leakage currents less than 0.1 A/cm^2 at temperatures above 900°C.

A wide variety of SiC devices have been demonstrated showing device functionality above 600°C. An excellent review of SiC device development is given by Casady and Johnson.[6] In summary, demonstrated SiC devices include the power MOSFET (400°C, 600-V, 1.8-A device), microwave metal-semiconductor field-effect transistor (400°C, 42 GHz), power junction field-effect transistor (500°C), power bipolar junction transistors (BJTs) (500°, $\beta \sim 5$–15), power thyristor (500°C, 2 kAcm^{-2}), and power p/n (600°C, 4.5-kV breakdown) and Schottky (700°C, 1-kV breakdown) diodes. It is noted that, although the SiC power device results look very promising, nearly all devices reported are very small in size (device area) and require significant scaling up to be of practical use in PMAD applications. The lack of high-quality defect-free SiC substrates and of suitable device passivation and gate dielectric materials has prevented development of larger power devices. However, excellent progress has been achieved in these areas in the last two to three years, and larger practical devices are currently in development.

Potential for Improved PMAD Efficiency Using WBG Devices

As mentioned, WBG-based electronic systems have good potential for reducing heat dissipation and, consequently, the required

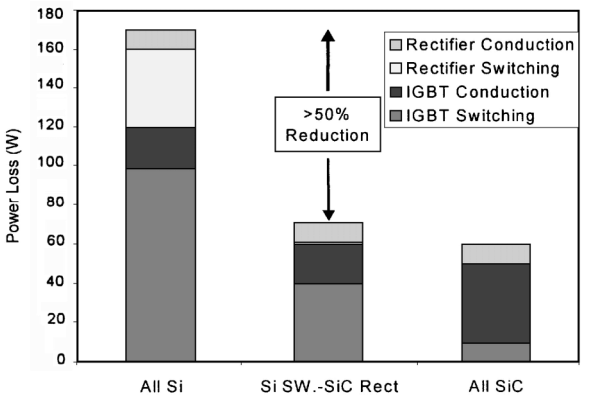


Fig. 9 Typical 400-V, 15-A motor circuit at 15 kHz; overall losses are reduced by 50% by using SiC.

electronics cooling capacity. Reduced heat dissipation results from increased device efficiency. WBG devices rival Si devices in efficiency through reduced conduction and switching losses. In the case of power devices, conduction losses depend on the thickness W (cm) and doping level N (particles/cm^3) of the semiconductor layers used for blocking reverse voltages; where conduction losses decrease with smaller W and larger N. In the case of a p/n junction, which is the fundamental voltage blocking structure in power switching devices, we find $W \propto E_C^{-1}$ and the maximum value of $N \propto E_C^2$. The value of E_C increases with semiconductor band gap approximately as $E_C \propto E_g^{3/2}$. Consequently, the ideal resistive conduction loss for power switching devices using 4H-SiC (the 4H refers to the crystal lattice structure within the device) with $E_g \sim 3.3$ eV will be less than 80 times that for Si devices with $E_g = 1.1$ eV. Similarly, WBG devices will exhibit lower switching losses than Si devices, which primarily depend on device size through the magnitude of device junction capacitance. Increasingly smaller geometry power switching devices can be designed using WBG materials because of increased current density (due to reduced conduction losses), resulting in smaller values for junction capacitance and lower switching losses. Because device conduction losses are inversely proportional to device area and device junction capacitance varies as device area, WBG devices can be made smaller to give reduced switching losses while maintaining conduction losses that are substantially lower than for Si devices. The impact of replacing Si-based power transistor and diode devices with SiC-based equivalent devices is shown in Fig. 9 for a generic 6-kW motor controller. A significant amount of the power savings results from replacing the Si pin diode with a SiC Schottky diode.

Conclusions

Recent development efforts at PRS in the area of EPS have shown that significant reductions in power management and distribution mass and volume can be achieved with greater dc–dc converter efficiency, operation at higher bus voltage and conversion frequency, and operation of the electronics at higher temperature. Today a typical satellite EPS accounts for about 20–30% of the total satellite mass, and the mass of PMAD electronics and harness (cabling and connectors) typically accounts for ~35–45% of the total EPS mass. Increased PMAD circuit efficiency will reduce the size of both the solar array and thermal control system through reduced power dissipation. Significant reductions in PMAD harness mass is achieved with higher PMAD bus voltages through reduced current conduction losses. Higher frequency PMAD circuit operation, which is enabled using high-speed devices made from advanced semiconductor materials such as GaAs, reduce the size and weight of transformers and filtering components. This feature, coupled with advanced compact packaging technologies result in reduced PMAD box mass and volume. Further, considerable potential exists for reducing the area of the thermal control radiator by a factor of >5 times using HT (200–250°C) PMAD components. The thermal analysis shows that for PMAD systems incorporating HT components, heaters used to maintain minimum operating temperature would not be required for worst-case cold environment, and the size of radiator components for hot environments would be reduced resulting in a substantial reduction in thermal radiator mass of 50 kg for LEO and almost 150 kg for GEO spacecraft. This progress is enabled by the development of WBG semiconductor devices, such as those made from SiC that demonstrate functionality above 500°C showing promise for reliable operation above 300°C. This compares with the maximum MIL-STD temperature of 125°C for Si-based power devices. The HT capability of WBG devices will also enable circuit use in locations where cooling is impractical such as in the 300°C thermal containment vessel of next-generation NaS batteries. Finally, the benefits of standardization of PMAD systems were recognized to minimize nonrecurring costs and cycle times for designs. These accomplishments will enable the design of future small satellites (<1000 W) and much larger monster satellites (10–50 kW) that demand reductions in satellite bus mass to enable greater payload mass and allow the use of smaller, less costly, and easier to deploy launch vehicles.

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A. C. Tribble
Associate Editor